REMARKS/ARGUMENT

The present Amendment is submitted for entry with an RCE. Claims 1-16 and 26 are pending after entry of this Amendment. Claims 1 and 10 are herein amended to positively recite that the carbon doped oxide layer is formed directly over and in direct contact with the inorganic dielectric layer/silicon dioxide layer. Applicants further amend claims 1 and 10 to clarify the present invention by positively reciting that the trench layer/carbon doped oxide layer is formed to define a metallization line layer, and that the silicon dioxide layer defines a via layer. Examiner is directed to page 10, line 21-page 11, line 5, page 12, lines 6-8, and Figures 2-6 for support of the claim amendments. No new matter is introduced.

In the Claims

Applicants have updated the status of claims 27-31 in accordance with revised amendment practice under 37 CFR §1.121. According to 37 CFR §1.121, a claim is "Withdrawn" if it is still in the application, but in a non-elected status. In Paper No. 4, a Restriction Requirement was imposed, and Applicants subsequently elected, with traverse, claims 1-16 and 26 in Paper No. 5. Claims 27-31 therefore technically remain in a non-elected status. In accordance with the Final Office Action of Paper No. 9, Applicants *proposed cancellation of claims 27-31 in accordance with Applicants' election of claims 1-16 and 26 in paper No. 5.* Applicants therefore submit the technically correct status of claims 27-31 is "Withdrawn," and Applicants retain the right to timely file a Divisional Application for the non-elected claims.

Rejections under 35 U.S.C. § 103

Claims 1-3, 7-10, and 14-15 were rejected under 35 U.S.C. §103(a) as being unpatentable over Parikh (U.S. Patent No. 6,225,207) in view of Yu et al. (U.S. Patent No. 6,187,663). Applicants respectfully traverse this rejection and request reconsideration.

Parikh teaches methods for ***triple*** and ***quadruple*** damascene fabrication. According to the Parikh reference, triple damascene structures are fabricated in five consecutive "dielectric" layers. As is discussed in greater detail below, two of the five layers are in fact etch stop layers. The

Parikh structures are fabricated using two etching sequences to form a power line trench, two signal line trenches, and vias. The power line trench, signal line trenches, and vias are filled to form triple and quadruple damascene structures.

Yu et al. teach a method for fabricating a copper damascene structure which includes two composite low-k dielectric layers each fabricated of two layers of low-k materials, and the two composite layers are separated by an etch stop layer of silicon oxynitride.

Applicants' independent claim 1, as amended herein, claims a method for making a dielectric structure for dual-damascene applications. Applicants' dual damascene method includes providing a substrate, fabricating metallization lines within the substrate, and then forming a barrier layer over the metallization lines and the substrate. Next, an inorganic dielectric layer to define a via dielectric layer is formed directly over the barrier layer. The inorganic dielectric layer has a dielectric constant of about 4, and is highly selective relative to the barrier layer when etched. The method then provides for forming a carbon doped oxide layer to define a trench dielectric layer over, and in direct contact with, the inorganic dielectric layer. The trench layer is formed to define a metallization line layer.

Applicants' independent claim 10, as amended, claims a method for making a multi-layer inter-metal dielectric over a substrate. The method includes forming a barrier layer over the substrate, and then forming a silicon dioxide layer over the barrier layer. The silicon dioxide layer has a dielectric constant of about 4. Next, the method provides for forming a carbon doped oxide layer directly over, and in direct contact with, the silicon dioxide layer. Then, a trench is formed through the carbon doped oxide layer, and a via is formed in the trench extending through the silicon dioxide layer to the barrier layer. The silicon dioxide layer defines a via layer and the carbon doped oxide layer defines a trench layer for metallization lines.

To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine the reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art references when combined, or as modified, must teach or suggest all the claim limitations.

(MPEP §2143). Applicants respectfully submit the Office has failed to establish a *prima facie* case of obviousness.

In paper 20, the Office provided no response to Applicants' Amendment of April 18, 2003, proclaiming the previous argument moot in view of new grounds for rejection. Applicants note, however, analogous argument in companion application 09/788,105, is applicable to the present application. Accordingly, Applicants have amended claims 1 and 10 to positively recite that carbon doped oxide layer is formed directly over and in direct contact with the inorganic dielectric layer/silicon dioxide layer.

Applicants further note that the Office is failing to appreciate the structure and substance of the presently claimed invention, and instead is apparently focused on individual features and elements. While Applicants recognize that such focus is necessary for effective examination, the resulting and claimed, entire structure and process must also be carefully considered. In the field of semiconductor devices, a number of structures, materials, processes, and so forth will be found common to both prior art and to inventive methods, processes, devices and systems. The present invention, as in many if not most inventions, does not lie in just the individual features of a claim. Applicants respectfully request meaningful examination of both the individual features as well as the overall process of the presently claimed method.

According to the Office, the Parikh reference teaches a method for making a multi-layer inter-metal dielectric structure as recited in Applicants' independent claims 1 and 10. Applicants point out that independent claim 1 recites a dielectric structure for dual-damascene applications, and Parikh is certainly not teaching dual-damascene. However, Parikh also does not teach or suggest Applicants' claimed invention. Citing Figure 4, and non-specifically the entire Parikh reference save the claims and the abstract ("col. 1-19"), the Office asserts that Parikh teaches Applicants' independent claims 1 and 10 except for the feature that the inorganic dielectric layer has a dielectric constant of about 4. In addition to suggesting that a range of a dielectric constant involves routine optimization, the combination with Yu et al. is asserted, apparently, to capture an inorganic dielectric of FSG having a dielectric constant of about 4.

The Office has identified layer 412 of Parikh as a barrier layer teaching Applicants' forming a barrier over the metallization lines and the substrate. In the Parikh reference at col. 9,

lines 30-42, layer 410 is identified as a substrate, and layer 412 as a first dielectric layer. Parikh has disclosed five "dielectric layers," of which two are etch stop layers. Layer 412 is described as a first dielectric layer, layer 414 as a second dielectric layer, layer 416 as a third dielectric layer, layer 418 as a fourth dielectric layer, and layer 420 as a fifth dielectric layer. Layers 414 and 418 are etch stop layers (col. 9, lines 38-39).

Next, the Office identifies layer 414 as an inorganic dielectric silicon dioxide layer to define a via dielectric layer directly over the barrier layer. As pointed out, layer 412 is not a barrier layer. Additionally, layer 414 is not a via dielectric layer, but an etch stop layer. Vias are etched through layer 414 underlying power line 450, and signal line 454, as well as through first dielectric layer 412 to substrate 410.

Next, the Office identifies layer 416 as a carbon-doped oxide layer to define a trench layer directly over the inorganic dielectric silicon dioxide layer. While the bottom of power line trenches 450 and 452 are in third dielectric layer 416, so too is via 456 underlying signal line 454. Applicants have amended claims 1 and 10 to further clarify that the carbon doped oxide layer defines a trench dielectric layer, and that the trench dielectric layer defines a metallization line layer. While Parikh contains a portion of metallization lines in a lower part of power lines 450 and 458, and contains via 456 traversing through third dielectric layer 416, Parikh's third dielectric layer 416 defines neither a trench layer, nor a trench layer to define a metallization line layer. In other words, power lines 450 and 458 extend into, and terminate in, third dielectric layer 416, but third dielectric layer 416 does not define a trench dielectric layer since it has both trenches and vias in the layer, and it does not define a trench layer to define a metallization line layer since it contains both metallization lines and metal vias through the layer, while the metallization lines are defined in at least three layers for power lines 450 and 458, assuming etch stop layer 418 is identified as a dielectric layer.

For at least the above reasons, Applicants respectfully submit that Parikh, and the combination of Parikh and Yu et al. fail to teach or suggest all of the claim limitations of Applicants' independent claims 1 and 10. Consequently, Parikh, and the combination of Parikh and Yu et al. fail to teach or suggest all of the claim limitations of Applicants' dependent claims 2-3, 7-9, and 14-15, each of which depends directly or indirectly from one of independent claims 1

and 10. The fact that all of Applicants' claim limitations are not found in the asserted combination establishes that the Office has failed to present a *prima facie* case of obviousness, and is not intended to address further issues of whether or not any motivation exists to assert such a combination. Applicants therefore request that this rejection be withdrawn.

Claim 26 was rejected under 35 USC §103(a) as being unpatentable over Parikh in view of Yu et al., as applied to claim 10, and further in view of Smith (US Patent No. 6,277,733). Applicants traverse this rejection and request reconsideration.

Smith teaches a barrier (422) over a conductor (420). A low dielectric constant layer (424) is formed over the barrier (422), and a hardmask (426) is formed over the low dielectric constant layer (424). Another low dielectric constant layer (430) is formed over the hardmask (426). While the hardmask (426) may be etched for via formation, when the vias are formed, the low dielectric constant layer (430) over the etched portion is removed (Fig. 2d). Therefore, Smith teaches a low dielectric constant layer over a hardmask over a low dielectric constant layer over a barrier over a substrate.

As described above, Applicants submit that the combination of Parikh in view of Yu et al. fail to teach or suggest all of the claim limitations of Applicants' independent claim 10. The additional combination of Smith fails to teach the claim limitations of independent claim 10 that the combination of Parikh in view of Yu et al. fail to teach, and even if Smith teaches additional claim limitations found in dependent claim 26, the combination still fails to teach all of Applicants' claim limitations. The fact that all of Applicants' claim limitations are not found in the asserted combination establishes that the Office has failed to present a *prima facie* case of obviousness, and is not intended to address further issues of whether or not any motivation exists to assert such a combination. Applicants therefore request the rejection of claim 26 be withdrawn.

Claims 1-4 and 7-16 were rejected under 35 USC §103(a) as unpatentable over Wang et al. (US Patent No. 6,077,574) in view of Usami (US Patent No. 6,077,574) and Yu et al. This rejection is traversed, and Applicants request reconsideration.

Wang et al. disclose a conductive layer (10) over which an etch stop layer (12) has been formed. A first dielectric layer (14) is formed over the etch stop layer (12), and a second dielectric

layer (18) is formed over the first dielectric layer (14). The second dielectric layer (18) is a low k dielectric material that is spin-coated on the first dielectric layer (14). Wang et al. describe the first dielectric layer (14) as formed of a low k dielectric material with a k value of less than 4 (see col. 5, lines 32-35), and the second dielectric layer (18) also being comprised of a low k dielectric material (col. 5, lines 55). The second low k dielectric material is disclosed to require a different sensitivity than the low k dielectric material in the first dielectric layer (14) to at least one etchant chemistry (col. 5, lines 60-63), although it is not disclosed that one or the other layer needs to have the lower of the two low k values.

Usami teaches a process for forming a plasma CVD fluorine-doped SiO_2 dielectric film in which a feed gas is supplied to a plasma CVD apparatus. The feed gas includes, among various gases, carbon and fluorine gases which are controlled independently of each other resulting in a silicon-based SiO_2 dielectric film doped with fluorine and carbon for a low dielectric constant value.

Wang et al., therefore, do not disclose forming an inorganic dielectric layer/silicon dioxide layer over a barrier, the inorganic dielectric layer/silicon dioxide layer having a dielectric constant of about 4, and forming a carbon doped oxide layer directly over, and in direct contact with, the inorganic dielectric layer/silicon dioxide layer. Wang et al. specifically teach a low k dielectric material of less than 4. While the Office has asserted that the k value of the dielectric material is one of routine optimization, the Office has overlooked that a k value of a dielectric material is of material importance to the formation of a semiconductor device or structure, and to the resulting structure so formed, which is well known in the art. The k value of a dielectric is not merely a parameter of, for example, temperature or concentration, and as is well known in the art, the selection of a low k dielectric or election not to use a low k dielectric defines and determines the material properties and function of the resulting structure or device. Applicants have specifically claimed a k value of the inorganic dielectric/silicon dioxide layer of about 4 to define a via layer to specifically claim that the via layer is ***not*** a low k dielectric layer. Wang et al. teach a low k dielectric layer.

Usami is asserted to be combined with Wang et al. in order to achieve a carbon doped oxide layer where Wang et al. teach a second dielectric layer (18) being a low k dielectric material that is

spin-coated on the first dielectric layer (14). Usami, however, does not teach or suggest an inorganic dielectric layer/silicon dioxide layer having a dielectric constant of about 4. Therefore, the combination of Wang et al. in view of Usami, still results in a low k dielectric layer over a low k dielectric layer and does not teach or suggest all of the claim limitations as recited in Applicants' independent claims 1 and 10, as amended herein. Applicants respectfully request this §103 rejection be withdrawn.

Claims 5-7 and 12-13 were rejected under 35 USC §103(a) as being unpatentable over Wang et al. in view of Usami and Yu et al., as applied to claim 4 and 11, and further in view of Applicants' admitted prior art. Applicants traverse this rejection and request reconsideration.

As described above, the combination of Wang et al. in view of Usami and Yu et al. fail to teach all of the claim limitations of Applicants' independent claims 1 and 10. Consequently the combination of Wang et al. in view of Usami and Yu et al. fail to teach all of the claim limitations of dependent claims 4 and 11, which depend from independent claims 1 and 10 respectively. Whether or not the use of TEOS is admitted prior art or known in the art does not establish a *prima facie* case of obviousness for claims 1 and 10, and therefore does not establish a *prima facie* case of obviousness for claims 5-7 and 12-13. Applicants request the rejection be withdrawn.

Claim 26 was rejected under 35 U.S.C. §103(a) as being unpatentable over Wang et al. in view of Usami and Yu et al as applied to claim 10 above, and further in view of Smith. Applicants respectfully traverse this rejection and request reconsideration.

As described above, the combination of Wang et al. in view of Usami and Yu et al. fail to teach all of the claim limitations of Applicants' independent claim 10. The additional combination of Smith fails to teach the claim limitations of independent claim 10 that the combination of Wang et al. in view of Usami and Yu et al. fail to teach, and even if Smith teaches additional claim limitations found in dependent claim 26, the combination still fails to teach all of Applicants' claim limitations. Applicants therefore request the rejection of claim 26 be withdrawn.

In view of the foregoing, Applicants respectfully request reconsideration of claims 1-16 and 26. Applicants submit that all claims are in condition for allowance. Accordingly, a notice of allowance is respectfully requested. If Examiner has any questions concerning the present Amendment, the Examiner is kindly requested to contact the undersigned at (408) 749-6900, ext. 6905. If any additional fees are due in connection with filing this amendment, the Commissioner is also authorized to charge Deposit Account No. 50-0805 (Order No. LAM1P106A). A copy of the transmittal is enclosed for this purpose.

Respectfully submitted,
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